REMARKS

Applicant has carefully reviewed and considered the final Office action and the cited references. Entry of the above noted amendments are respectfully requested. Claims 1-4, 6, 8, 10-11, 13, and 15 have been amended. Claim 5 has been cancelled without prejudice. New claims 16-19 have been added.

SUPPORT FOR NEW CLAIMS ADDED

It is respectfully submitted that the new claims are supported by the present application as filed in the Patent and Trademark Office, that the new claims satisfy the written description requirement and the other requirements of 35 U.S.C. §112, and that no new matter is being added.

CLAIM REJECTIONS – 35 U.S.C. §112

Claims 2, 4, 8 and 13 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention as well as for being misdescriptive. In response to the rejection of claims 2, 4, 8 and 13, applicant has amended claims 2, 4, 8 and 13 to more clearly describe the invention recited in those claims without adding any new matter.

Claims 3, 11 and 14 are rejected because of an alleged discord with the embodiment disclosed in FIG. 2. Claims 3, 11 and 14 recite that the delay circuits respectively receive the output signals of the off-chip drivers. This configuration is clearly shown in FIG. 9, which applicant filed in an amendment with the United States Patent and Trademark Office on March 14, 2005. Specifically, FIG. 9 shows that the delay circuits respectively receive the output signals of the off-chip drivers. Furthermore, this configuration is disclosed in page 7, lines 13-18 of the specification. Therefore, applicant respectfully submits that claims 2-3, 4, 8, 11, and 13-14 are in condition for allowance and request that the rejections under 35 U.S.C. §112, second paragraph be withdrawn.

CLAIM REJECTIONS – 35 U.S.C. §102

Claims 1-15 are rejected under 35 U.S.C. §102(b) as being anticipated by Watkins et al. (US Pat. 6,359,483). In addition, claims 1, 3 and 5 are rejected under 35 U.S.C. §102(b) as being anticipated by Hirasaka (US Pat. 6,134,691).

Independent claims 1, 3, 6 and 11, as amended, recite an off-chip driver circuit having a plurality of off-chip drivers and a plurality of delay circuits. The off-chip drivers respectively receive data signals (or delayed data signals) and generate respective output signals in response to respective control signals. The delay circuits receive the respective output signals (or the data signals) and generate delayed output signals (or delayed data signals), respectively.

Furthermore, the off-chip driver circuits recited in amended claims 1, 3, 6 and 11 further disclose that the total number of the off-chip drivers to be activated at the same time is changed by the respective control signals which are generated in response to a desired drivability. In addition, the activated off-chip drivers sequentially generate the output signals in response to the delay times of the delay circuits so that a total drivability of the off-chip driver circuit increases to the desired drivability.

However, the cited references do not disclose or suggest that the off-chip drivers are activated at the same time by the control signals. In contrast, Watkins discloses in FIG. 2 a plurality of NAND gates 142 to 156 that are activated sequentially. In addition, only one of NAND gates is ever activated at a given time. In other words, nowhere does Watkins disclose activating more than one off-chip driver at the same time.

The invention recited in independent claims 1, 3, 6 and 11, as amended are generally directed to a circuit to control drivability, such that data signals output from an off-chip driver circuit do not undergo turn on/off at the same time at a high frequency state by giving different delay times to the data signals input into the off-chip drivers. In contrast, Watkins generally discloses a circuit to control delay time of a clock signal for the purpose of synchronization. Therefore, the circuit disclosed in Watkins is directed to completely unrelated subject matter as that of the claimed invention, and those of ordinary skill in the art would not have looked to Watkins to derive the structures found in amended claims 1, 3, 6 and 11.

Likewise, in FIG. 5 of Hirasaka, a plurality of selectors S0 to S2 are activated selectively. In addition, Hirasaka does not appear to disclose simultaneously activating more than one of selectors at the same time.

Furthermore, the cited references merely disclose controlling a delay time of a signal as a clock signal. It is thus submitted that the cited references do not disclose or suggest that a total drivability of the off-chip driver circuit increases by controlling the number of the off-chip drivers to be activated.

Accordingly, applicant believes that the claim 1, 3, 6 and 11, as well as the claims dependent thereon, are distinguishable from Watkins and Hirasaka. In view of the above amendments and remarks, applicant believes the pending application is in condition for allowance, and respectfully requests that a timely Notice of Allowance be issued in this case.

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Respectfully submitted,

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